# ELEC 374 Quiz 4 – Testability

**Fault Cause**

* As VLSI technology advances the chance of producing a faulty product increases
* Causes of faults
  + Inconsistent system specifications
  + Unreliable system clocking
  + Design rule violations
  + Logical design errors
  + Faulty devices
    - Shorted wires, bad contact, incorrect doping etc.
  + Incorrect wiring and interconnection

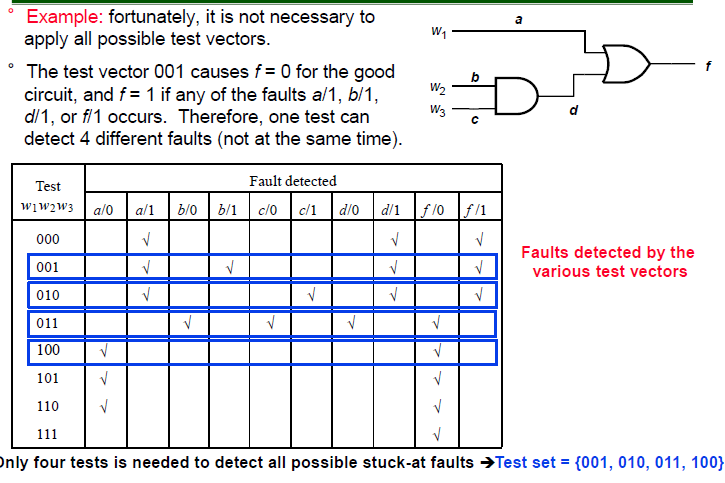
**Fault Modelling**

* Fault Model
  + Idea of how circuit might behave
  + A test pattern is generated from the fault model
    - It will detect defaults when the faulty circuit behaves the same as the pattern predicted by the fault hypothesis
* Stuck at fault model
  + Some defects cancause a logic signal to become connected to the power rails. The fault will be permanently stuck at 1 or 0
  + A wirte w, that has an undesirable signal that always corresponds to the logica value 0 is stuck at 0
  + A wirte w, that has an undesirable signal that always corresponds to the logica value 1 is stuck at 1
  + Single stuck at fault model
    - Assumes that only one stuck at fault can occur
  + A fault is detected if the outputof the circuit is different from the value produced by the good circuit when an appropriate test is applied as input
  + Test vector set
    - Each test is supposed to be able ro detect the occurrence of one or more faults. A complete set of tests for a given circuit is referred to as the test set

**Terminology**

* **Fault detection**
  + The test vector detects the fault
* Fault location
  + Location of the fault is known
* Controllability
  + An input to a device under test is called the primary input
* Observability
  + Indicates the relative difficulty of propagating an error from a wire to a primary output
* Fault simulation
  + Determines the effect of an assumed faulet on the behaviour of the circuit.
* Fault diagnosis
  + Upon fault simulation, a database is built relating the test pattern and the location or type of the fault. Fault diagnosis uses several test patterns to obtain several responses. Fault is located based on some decision
* Fault coverage
  + The ratio of detected faults to the total number of assumed faults

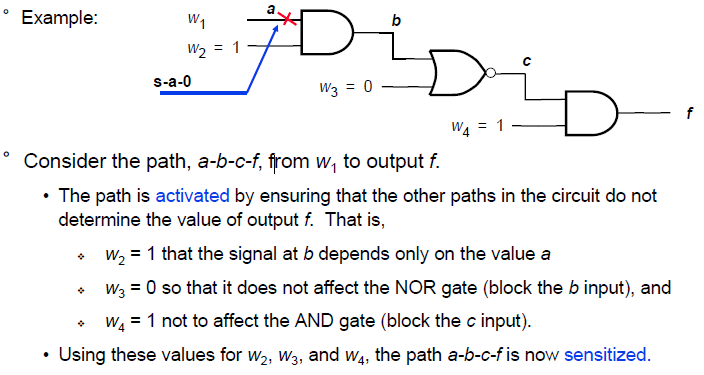
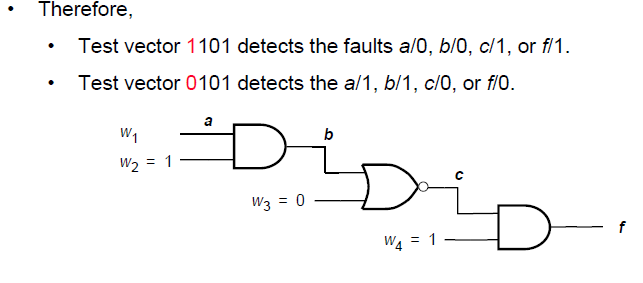
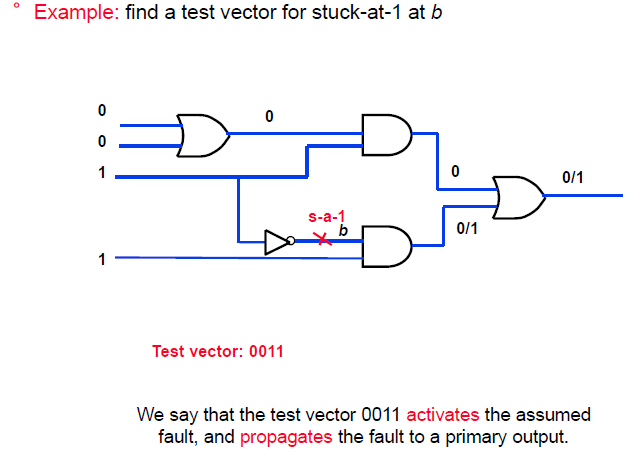
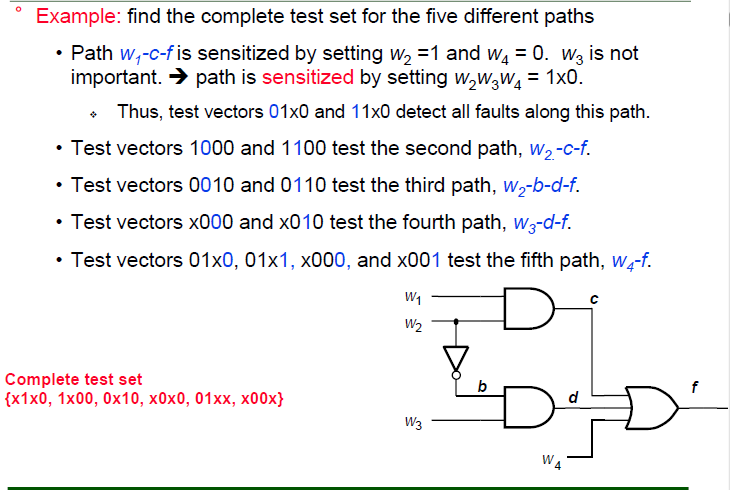
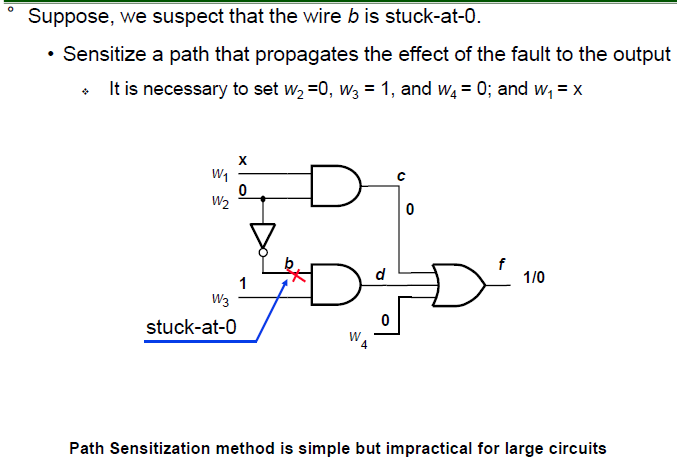
**Test Set Complexity**

* **Exhausive testing**
  + We can make sure that the digital circuit behaves properly by applying all input patterns and compare the outputs with the expected outputs
* Combinational circuit testing
  + For a combinational circuit with n inputs and m outputs we need 2n input test vectors and the corresponding 2m output vectors
* Sequential circuit testing
  + Difficult to test the sequential circuits because the behavior of the circuit under test is influenced by the states that the circuit is in when the tests are applied
  + For a sequential circuit with k feedback lines the exhaustive test requires 2n+k test vectors
* 

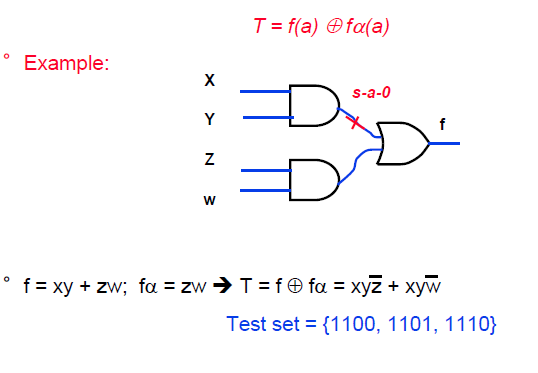
**Automatic test pattern generation for combinational circuits**

* It is required to obtain test patterns to the inputs of the logic circuit under test such that the presence of a fault can be observed at the output
* Several techniques for determining the test patterns will be discussed next

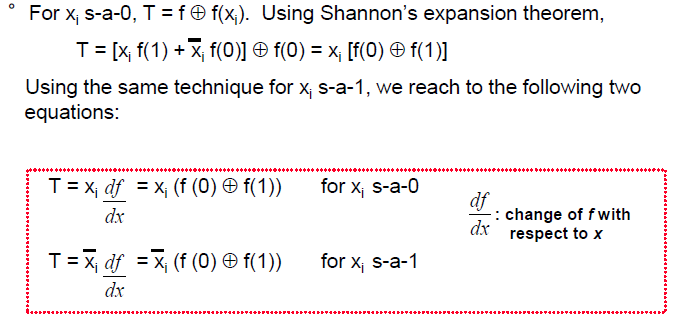
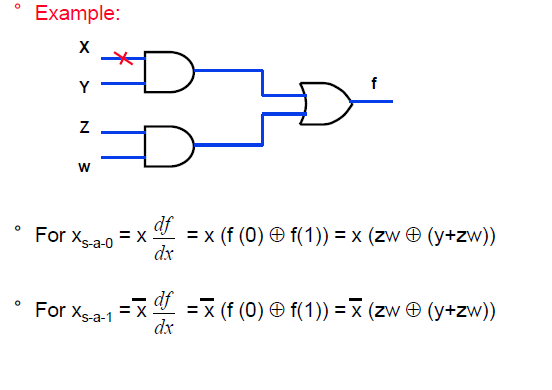
**Path sensitization method**

* Path sensitization
  + The size of the test set is normally much smaller than 2^n but it may still be impractical. The better approach is to deal with several wires that form a path as an entity that can be tested for several faults using a single test
* 
* 
* Path sensitization rules
  + To sensitize a path through an input of AND or NAND gate all other inputs must be set to 1
  + To sensitize a path through an input of an OR or NOR gate all other inputs must be set to 0
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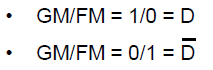
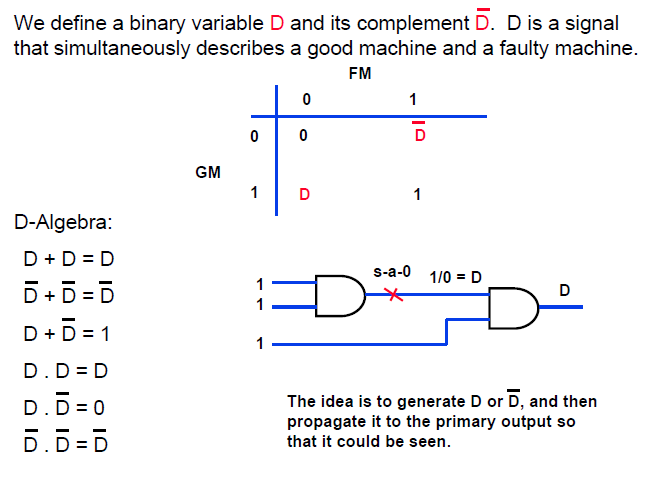
**Test Function Method**

* Test function
  + IF f(a) is a function for the good machine, and f alpha(a) the function for the faulty machine , then f(a) != f alpha(a) for an input a
  + 

**Boolean Difference Method**

* Shannon’s Expansion Theorum
  + Any Boolean function f(x1, …., xn) can be written in the form
  + 
* 
* 

**D Algorithm**

* D Algorithm considers two machinesL a good machine (GM) and a faulty machine (FM) in which a single fault occurs
* A five valued logic is used to represent logic signals for both machines. The signals could have the values 0, 1, x, D, Dnot
  + 
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